

What is claimed is:

Sub A27  
1. An equalizer circuit comprising:

2 carrier sensing means for sensing the start of a  
3 reception signal on the basis of a signal representing a  
4 reception level of the reception signal;  
5 first and second equalizing means for equalizing the  
6 reception signal;  
7 control means for alternately enabling said  
8 first and second equalizing means every frame reception  
9 in accordance with an output from said carrier sensing  
10 means; and  
11 switching means for alternately switching  
12 between outputs from said first and second equalizing  
13 means every frame reception and outputting the selected  
14 output as demodulation data.

2. A circuit according to claim 1, wherein

2 said control means alternately outputs first  
3 and second carrier sense signals to said first and  
4 second equalizing means for a time interval from time  
5 when the detection signal is output from said carrier  
6 sensing means to time when equalizing processing is  
7 complete in said first and second equalizing means, and  
8 said first and second equalizing means  
9 alternately equalize the reception signal every frame  
10 reception in response to first and second carrier sense

11 signals from said control means.

3. A circuit according to claim 2, further  
2 comprising first and second gate means for receiving a  
3 system clock signal and the first and second carrier  
4 sense signals from said control means and supplying an  
5 output clock signal to said first and second equalizing  
6 means.

4. A circuit according to claim 2, wherein  
2 said first and second equalizing means output  
3 first and second demodulation data used during  
4 equalizing processing to said switching means and output  
5 first and second demodulation data gate signals  
6 synchronized with the first and second demodulation data  
7 to said control means and said switching means,  
8 said control means stops outputting the first  
9 and second carrier sense signals in response to the  
10 first and second demodulation data gate signals, and  
11 said switching means alternately outputs the  
12 first and second demodulation data in response to the  
13 first and second demodulation data gate signals.

5. A circuit according to claim 2, wherein  
2 said first and second equalizing means  
3 comprise equalizers for setting tap coefficients and  
4 memories for storing preamble signals of the reception

5 signal, and

6 said first and second equalizing means detect  
7 frequency offset values, estimate transmission line  
8 characteristics, and set the tap coefficients at the  
9 start of reception of the reception signal.

6. An equalizing method comprising the steps  
2 of:

3 detecting the start of a reception signal on  
4 the basis of a signal representing a reception level of  
5 the reception signal;

6 alternately enabling first and second  
7 equalizer units for equalizing the reception signal upon  
8 detecting the start of the reception signal; and

9 alternately switching between outputs from  
10 said first and second equalizer units every frame  
11 reception and outputting the selected output as  
12 demodulation data.

7. A circuit according to claim 4, wherein the  
2 step of alternately enabling further comprises the step  
3 of alternately outputting first and second carrier sense  
4 signals as enable signals to said first and second  
5 equalizer units for a time interval from time when the  
6 start of the reception signal is detected to time when  
7 equalizing processing is complete in said first and  
8 second equalizer units.

8. A circuit according to claim 5, further  
2 comprising the step of alternately supplying a system  
3 clock signal to said first and second equalizer units in  
4 accordance with the first and second carrier sense  
5 signals.

Add A27